REMARKS / ARGUMENTS

This reply is responsive to an Office Action dated March 17, 2004.

In the specification, the paragraphs [0026] and [0048] have been amended to correct minor editorial problems. In this regard, the two paragraphs have been amended to delete the term "t." Also, in paragraph [0048], the value of Db was corrected to be consistent with the value shown for it in FIG. 5.

Claims 1 – 12 remain in the application. New claims 13 – 17 have been added. Claims 1, 2, 4, 5 and 7 – 11 have been amended.

The amendments to the claims were made to render them more clear and definite and to emphasize the patentable novelty thereof. There is no intent to surrender equivalence.

An Information Disclosure Statement accompanies this Reply and Amendment.

Specification

The specification has been objected to under 37 CFR 1.71 concerning paragraphs [0026] and [0048], relating to the terms Dr being equal to 2Db(t), where Db is the depth of an electronic component, and t is the thickness of the power distribution unit. It is noted with appreciation that the Examiner has pointed out that the term (t) should not be included, since Dr has a dimension of length and not a dimension of area. The depth of the rack housing Dr is defined in paragraph [0041] in the specification as being "approximately double that of Db."

The specification has been amended to clarify the disclosure. Specifically, the reference to "t" has been omitted so that the equation describes

"Dr" as now being equal to approximately "2Db." No new matter has been entered.

Claim Rejections – 35 USC § 112

Claim 2 has been rejected under 35 USC § 112, first paragraph, as failing to comply with the enablement requirement. The office action states that in claim 2, the depth of the rack housing Dr is equal to 2 Db(t), where Db is the electronic component, and t is the thickness of the power distribution unit. The office action points out that Dr has a dimension of a length and Db(t) has a dimension of an area and that they cannot be equal.

Therefore, Claim 2 has been amended to remove references to the term (t) to be consistent with the specification. See paragraph [0041] of the specification. Claim 1 has also been amended to include a reference to Dr as being "equal to approximately 2Db."

Claim 10 has been rejected under 35 USC § 112, first paragraph, as failing to comply with the enablement requirement. The office action states that "In claim 10, 'the lower one of said openings is located at a height Hh equal to 0.46 inch' needs a reference point for locating the opening."

Therefore, Claim 10 has been amended to include reference information for locating the opening, "wherein Hh is defined as the distance between the geometric center of the lower one of the openings and the outer surface of the bight portion of one of the lower component guides." This description is consistent with FIG. 8 of the drawing.

Therefore, amended claims 2 and 10 are now clear and definite, and comply with the enablement requirement.

Claim Rejections – 35 USC § 103

Claims 1 – 12 have been rejected under 35 USC § 103(a) as being unpatentable over Casanova et al. (US 5,031,075).

Casanova discloses a double-sided central electronics complex ("CEC") for increasing logic card density in a logic cage. Two logic cages are integrated, sharing one backplane so that the logic elements may be plugged into the CEC from both sides.

However, it is noted that Casanova teaches the use of logic elements mounted in CECs, and not the use of a rack assembly. In other words, Casanova teaches mounting logic cards in CECs, which then may be, in turn, mounted in conventional racks. Whereas Applicants claim an electronic component rack assembly, which does not include CECs.

In the Office Action, there is stated that a "change in size is generally recognized as being within the level of ordinary skill in the art." However, as specified in claims 1 and 2 as amended, Applicants' rack assembly employs a width Wr of "about 24 inches," and a depth Db "equal to approximately 2Db." These dimensions have been discovered by Applicants to be critical to achieve a very high density of computing power and yet be designed to be used conveniently in a conventional computer room setting.

The critical dimension of "about 24 inches" in width facilitates alignment of the rack assembly with floor vents in conventional computer rooms. By utilizing the critical width of "about 24 inches," Applicants' rack assembly can be readily aligned with conventional computer room floor tiles, and thus be automatically aligned with floor cooling vents to permit the rack assembly to be cooled by the cold air flowing from the vent.

If critical depth dimension of approximately two times the depth of each electronic component enables the "side-by-side upright" mounting arrangement for the "electronic components" in a back-to-back approximate registration" to substantially occupy the entire space within the rack assembly with little or no wasted space. Also, such a depth dimension enables Applicants' rack assembly to fit conveniently within the floor space of the conventional computer room. In this regard, similar or like rack assemblies can be readily spaced apart for convenient access by users.

In short, the critical width and depth dimensions of Applicants' rack assembly results in a unique high density computing unit, which fits conveniently within the confines of a conventional computer from floor design in proper alignment with floor vents. At the same time, the interior of the rack assembly has little or no wasted space. Thus, these critical dimensions produce a very high density computing system, which fits conveniently within existing floor requirements.

It is the intent of the Applicant's claimed approach to achieve a high density of computing power by fitting many computing components into a defined space. It is therefore undesirable to have little or no wasted space within the rack since wasted space lowers the overall computing power density.

As disclosed by the Applicant, typical computer rooms housing rack mounted computers are conventionally designed with floors having about 24 inches square tile which include spaced-apart air vents for cooling rack mounted computers. It is therefore highly desirable, and in most cases required, to comply with this floor specification in order to provide a rack mounted computer system to consumers of this technology.

A high amount of computing density is provided within the claimed critical width dimension under the Applicants' approach since the blades are mounted back-to-back in a unique and non-obvious technique where a rack depth "equal to...approximately 2Db" may be successfully achieved. The Applicant's claimed approach eliminates wasted space found in Casanova logic cages.

This form factor is unique and non-obvious and is neither taught nor suggested by Casanova. Casanova does not teach nor suggest forming a rack assembly "a width...about 24 inches" and "wherein the depth of the rack housing is equal to...approximately 2Db." In fact, Casanova teaches away from this concept by disclosing that the daughter boards are plugged into a double-sided backplane assembly 38 shown in Fig. 3 of the Casanova disclosure. Fig. 3 of Casanova shows a backplane assembly that appears to include at least five layers of circuit boards and connectors. The Casanova's technique is incapable of ever achieving a rack depth "equal to...approximately 2Db" as claimed by the Applicant.

Casanova clearly teaches away from saving space. See column 4, lines 13 – 51 where Casanova describes that when the logic elements are plugged into the CEC from both sides, the set of logic elements on one side of the backplane card are offset or staggered from the set of logic elements plugged in on the reverse side of the backplane card by one half of the width of a single card. In other words, the set of cards disposed on each side of the backplane are non-symmetric and offset with respect to each other, and already are not disposed "in a back-to-back approximate registration." Since the cards on each side of the Casanova backplane are non-symmetric, an offset, or wasted space, is then created between the sides of the cage and each row of cards. This phenomenon is shown in Fig. 4 of Casanova as offset "A" which indicates wasted space between the side of the cage and the top row of cards.

Casanova's offset approach leads to wasted space that decreases computing density. Thus, there is no teaching nor suggestion to use Casanova's technique to achieve the high computing density "electronic component rack assembly" as claimed by the Applicant where the critical depth of the rack assembly is "equal to approximately 2Db" and where the rack assembly has a critical width of "approximately 24 inches."

For the above reasons, claims 1 through 17 patentably distinguish over Casanova.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

By [signature]

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